What is Claimed Is:

1. A multiport data communication system for switching data packets between ports, the data communication system comprising:

a plurality of receive ports for receiving data packets,

a decision making engine responsive to the received data packets for controlling transmission of the received data packets to at least one selected transmit port,

the decision making engine including:

a plurality of queuing devices corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,

logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet, and

a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports.

2. The system of claim 1, wherein the scheduler is configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

3. The system of claim 2, wherein each of the plurality of the queuing devices is assigned with at least one of the time slots in each scheduling cycle.

4. The system of claim 3, wherein the scheduler is configured to allocate a first time slot assigned to a first queuing device to a second queuing device if no request for a time slot is received from the first queuing device.

5. The system of claim 4, wherein the second queuing device is assigned with a second time slot following the first time slot.

6. The system of claim 5, wherein the scheduler is configured to allocate the first time slot to a third queuing device if no request for a time slot is received from the second queuing device.

7. The system of claim 6, wherein the third queuing device is assigned with a third time slot following the second time slot.

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8. The system of claim 1, wherein the logic circuitry comprises ingress rules logic for receiving the data block to check whether the corresponding data packets are received with an error.

9. The system of claim 8, wherein the logic circuitry further comprises source address lookup logic for comparing a source address of the data packets with a preset source address.

10. The system of claim 9, wherein the logic circuitry further comprises destination address lookup logic for comparing a destination address of the data packets with a preset destination address.

11. The system of claim 10, wherein the logic circuitry further comprises egress rules logic for producing a port vector identifying the at least one selected transmit port.

12. In a communication system having a plurality of receive ports, at least one transmit port, and a decision making engine for controlling data forwarding between the receive port and the at least one transmit port, a method of data processing comprising the steps of:

placing data blocks representing received data packets in a plurality of data queues corresponding to the plurality of the receive ports,

transferring the data queues in successive time slots to logic circuitry for determining the at least one transmit port, and

dynamically allocating the time slots to the data queues in accordance with data traffic at the corresponding receive ports.

13. The method of claim 12, wherein a data queue representing each of the receive ports is assigned with at least one of the time slots.

14. The method of claim 13, wherein a first time slot assigned to a first data queue is allocated to the first data queue if the first data queue contains data to be processed.

15. The method of claim 14, wherein the first time slot is allocated to a second data queue if the first data queue does not contain data to be processed.

16. The method of claim 15, wherein the second data queue is assigned with a second time slot following the first time slot.

17. The method of claim 16, wherein the first time slot is allocated to a third data queue if the first and second data queues do not contain data to be processed.

18. The method of claim 17, wherein the third data queue is assigned with a third time slot following the second time slot.